UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/769,929	01/24/2001	Bhanu Nanduri	ALNC-9001 [P-6080]	5472

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EXAMINER
MATTIS, JASON E

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	**Applicant(s)**
Office Action Summary	09/769,929	NANDURI ET AL.
	Examiner	**Art Unit**	
	Jason E Mattis	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>04 October 2004</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is

closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-5</u> is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-5</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>04 October 2004</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some * c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage

   application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
      Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
      Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   This Office Action is in response to the amendment filed on 10/04/04. Due to the

amendments, objections to the drawings have been withdrawn. Claims 1-5 are

currently pending in the application.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   Claims 1-3 rejected under 35 U.S.C. 102(e) as being anticipated by Sang et al.

(U.S. Pat. 6577636).

With respect to claim 1, Sang et al. discloses a switch router circuit **(See**

column 4 lines 33-46 and item 12 in Figure 2 of Sang et al. for reference to a multi-

port switch 12). Sang et al. also discloses a plurality of Media Access Control units

(See column 4 lines 33-46 and items 20 in Figures 1 and 2 of Sang et al. for

reference to media access control units 20). Sang et al. further discloses each MAC

unit connected to a data bus for receiving incoming data packets from the data bus **(See**

Figure 2 of Sang et al. for reference to data bus 69 being connected to each of the

12 MAC units, which are represented by item number 20). Sang et al. also discloses

each incoming data packet including a packet header and a packet payload, with the

packet header identifying a destination port to which the packet payload is to be

transferred **(See column 5 lines 28-41 of Sang et al. for reference to a unit that**

"snoops" a data bus to determine the header information of a received packet

including destination address information, which means that the packets must

have a head with a destination address that identifies a destination port to which

the payload is to be transferred to). Sang et al. further discloses a controller

connected to the MAC units to receive the incoming packets therefrom **(See column 4**

lines 33-46 and item 40 in Figure 2 of Sang et al. for reference to decision making

engine 40 that is connected to the MAC units via bus 69 to receive incoming

packets). Sang et al. also discloses for each incoming data packet the controller

separating the packet header of the data packet from the packet payload of the data

packet **(See column 5 lines 28-52 of Sang et al. for reference to IRC 40 separating**

the data packet head from the data packet payload). Sang et al. further discloses a

lookup table connected to the controller to receive packet headers therefrom **(See**

column 14 lines 15-31 of Sang et al. for reference to IRC 40 including an address

table 82). Sang et al. also discloses that the lookup table utilizes a packet header to

determine whether the destination port identified by the packet header is included within

the plurality of MAC units of the switch router circuit **(See column 17 lines 19-42 of**

Sang et al. for reference to IRC 40 using the packet header and the address table

82 to determine which output port to forward the packet, which means that it

determines if the destination port is one of the MAC units of the switch and

routes the packet to the destination port). Sang et al. further discloses a multi-port

store/switch memory array connected to receive packet payloads of incoming data

packets **(See column 4 lines 47-63 and Figures 1 and 2 of Sang et al. for reference**

to an external memory 36). Sang et al. also discloses that the multi-port store/switch

memory array includes a plurality of storage areas with each storage area being

associated with a corresponding MAC unit such that a packet payload of an incoming

data packet received by the MAC unit is stored in the corresponding storage area of the

multi-port store/switch memory array **(See column 6 lines 54-67 of Sang et al. for**

reference to packets received by the MAC modules being sent to a storage area in

the external memory 36 and for reference to each of the storage areas of the

external memory being associated with each of the MAC modules using frame

pointers, which link a MAC unit to the area in which a received packet has been

stored in the external memory 36). Sang et al. further discloses an arbitrator

connected to the multi-port store/switch memory array **(See column 4 lines 33-46 and**

item 42 in Figure 2 of Sang et al. for reference to a switching subsystem 42, which

acts as an arbitrator, connected to the external memory 36 through bus 69). Sang

et al. also discloses that the arbitrator, in the event that the destination port identified by

the packet header of an incoming data packet is included within the plurality of MAC

units of the switch/router circuit, arbitrates direct connection of the memory array

storage area associated with the MAC unit that receives the incoming data packet to the

MAC unit identified as the destination port, thereby facilitating direct transfer of the

packet payload of the incoming data packet to the destination port **(See column 5 line**

53 to column 6 line 12 and column 7 line 51 to column 8 line 12 of Sang et al. for

reference to the switch subsystem 42 providing arbitrating a direct connection to

send the packet payload from the external memory 36 to the transmit FIFO

memory of the corresponding identified destination port or ports, meaning that

the switch subsystem 42 facilitates a direct connection of the packet payload

from the associated memory location of the MAC that received the packet to the

transmit FIFO memory corresponding to the destination MAC port and for further

reference to transferring the packet payload data using a direct memory access

(DMA) from the external memory 36 to the identified transmit FIFO memory).

With respect to claim 2, Sang et al. discloses that each of the storage areas in

the multi-port store/switch memory array includes a plurality of pass gates, one pass

gate being associated with a corresponding one of the MAC units **(See column 6 line**

54 to column 8 line 12 and Figure 3 of Sang et al. for reference to the method by

which the memory is accessed using pointers that are associated with

corresponding MAC units to access specific memory areas, which means there

must be a pass gate associated with each memory area so that the data my be

transferred by each memory area to a corresponding destination area). Sang et

al. further discloses each of the plurality of storage areas further including a storage

element such that the arbitrator arbitrates the pass gates of the incoming storage area

to the pass gates of the outgoing storage area whereby the packet payload is

transferred directly from the data storage element of the incoming storage area to the

data storage element of the outgoing storage area **(See column 7 line 51 to column 8**

line 12 and Figure 3 of Sang et al. for reference to the elements of switching

element 42 facilitating the transfer of a data payload from the external memory 36

to a transmit FIFO using a direct memory access (DMA), which is a memory

corresponding with the destination address of the payload, such that there is a

direct transfer of the payload from the incoming memory location in the external

memory 36 to the outgoing transmit FIFO memory area of the destination MAC

port).

  With respect to claim 3, Sang et al. discloses that the arbitrator arbitrates direct

connection of the memory array storage area associated with the MAC unit that

receives the incoming data packet to multiple MAC units identified as destination ports,

thereby facilitating multicasting of the packet payload to multiple destination ports **(See**

column 6 line 54 to column 8 line 26 and Figure 3 of Sang et al. for reference to

the elements of switching element 42 facilitating the transfer of a data payload

from the external memory 36 to a transmit FIFO, which is a memory

corresponding with the destination address of the payload, such that there is a

direct transfer of the payload from the incoming memory location in the external

memory 36 to the outgoing transmit FIFO memory area of the destination MAC

port and for further reference to a multicopy, or multicast, transmission of the

payload to multiple destinations being facilitated when multiple destinations are

designated by the packet header).

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sang et

al. in view of Poteet et al. (U.S. Pat. 4630240) and in further view of Bansal et al. (U.S.

Pat. 6650637).

With respect to claim 4, Sang et al. does not disclose that the multi-port

store/switch memory array facilitates double-ended write of incoming packets.

Poteet et al., in the field of communications, discloses the use of double ended

write in a memory system **(See column 7 lines 11-18 of Poteet et al. for reference to**

a dynamic memory including a double-ended write operation). Using a memory

with double ended write has the advantage of allowing for less memory write errors

since two write signals must be used to activate the write function.

It would have been obvious to one of ordinary skill in the art at the time of the

invention, when presented with the work of Poteet et al., to combine the use of the

double-ended write operation of Poteet et al. with the memory and switch of Sang et al.,

with the motivation being to allow for less memory write errors since two write signals must be used to activate the write function.

Sang et al. also does not disclose that the multi-port store/switch memory array facilitates buffered multi-port read of outgoing packet payloads.

Bansal et al., in the field of communications, discloses the use of buffered multi-port read of outgoing packet payloads **(See column 3 lines 11-23 of Bansal et al. for reference to the use of a buffered multi-port read operation in a multi-port RAM).** Using a memory with buffered multi-port read has the advantage of allowing multiple read functions as well as write functions to be carried out during a single memory clock cycle.

It would have been obvious to one of ordinary skill in the art at the time of the invention, when presented with the work of Bansal et al., to combine the use of buffered multi-port read as suggested by Bansal et al. with the memory and switch of Sang et al. and Poteet et al., with the motivation being to allow multiple read functions as well as write functions to be carried out during a single memory clock cycle.

6.   Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sang et al. in view of Majos et al. (U.S. Pat. 5640366).

With respect to claim 5, Sang et al. does not disclose that the multi-port store/switch memory array facilitates double port write of incoming packets and buffered double port read of outgoing packets.

Majos et al., in the field of communications, discloses a memory using double

port write and double port read **(See column 5 lines 22-35 of Majos et al. for**

reference to a double port random access memory with both double port write

and double port read operations). Using a memory with double port read and double

port write has the advantage of allowing multiple read functions as well as write

functions to be carried out during a single memory clock cycle.

It would have been obvious to one of ordinary skill in the art at the time of the

invention, when presented with the work of Majos et al., to combine the use of double

port write and read functions as suggested by Majos et al. with the memory and switch

of Sang et al., with the motivation being to allow multiple read functions as well as write

functions to be carried out during a single memory clock cycle.

Response to Arguments

7.   Applicants' arguments filed 10/04/04 have been fully considered but they are not

persuasive.

In response to the Applicants' argument that:

"Specifically, nothing in the cited section of the Sang et al. reference either

teaches or suggests a multi-port store/switch memory array that includes a

plurality of distinct storage areas wherein each specific storage area is

associated with a corresponding specific MAC unit." (See page 5 of

Applicants' Remarks)

the Examiner respectfully disagrees. The limitation in claim 1 regarding the multi-port

store/switch memory array calls for a "memory array including a plurality of storage

areas". The external memory 36 of Sang et al. meets this limitation since the external

memory has a plurality of addressed storage areas (See column 4 lines 53-58 of Sang

et al. for reference to the external memory having a 64-bit wide data path, with each

data path corresponding to a storage area, and a 17-bit wide address path, with each

address corresponding to one of the data paths). The addressable data paths make up

the claimed "plurality of addressed storage areas". The limitation in claim 1 regarding

the multi-port store/switch memory array also calls for "each storage area being

associated with a corresponding MAC unit such that a packet payload of an incoming

data packet received by a MAC unit is stored in the corresponding storage area of the

multi-port store/switch memory array". In the switch of Sang et al., when a MAC module

receives incoming data, it uses a queuing logic 74 to fetch a frame pointer from the free

buffer queue 64 (See column 6 lines 57-64 of Sang et al.). The frame pointers of Sang

et al. specify the location in the external memory 36 where the received data frame will

be stored (See column 6 lines 64-67 of Sang et al.), meaning the pointer points to an

addressed storage area of the external memory 36. Further, since the fetched frame

pointer is now removed from the free buffer queue 64, this frame pointer associates the

addressed storage area of the external memory 36 with the MAC module that fetched

the frame pointer. Therefore, by having the MAC units fetch pointers to addressed

storage areas of the external memory 36, the storage areas of the external memory 36

are dynamically associated with the corresponding MAC modules that fetched the

pointers, and incoming data received at the MAC modules is stored in the storage areas

specified by the pointers. There is no limitation in claim 1 that precludes the storage

areas of the memory array from being dynamically allocated to corresponding MAC

units as is done by Sang et al. Thus, Sang et al. discloses all the limitations of claim 1

regarding the "multi-port store/switch memory array".

> In response to the Applicants' argument that:

>> "Further, nothing in the Sang et al. reference either teach or suggests an
>> arbitrator that arbitrates direct connection of the specific memory array
>> storage area associate with MAC unit that receives the incoming data
>> packet to the specified MAC unit identified as a destination port by the
>> packet header of the data packet". (See page 5 of Applicants' Remarks)

the Examiner respectfully disagrees. As discussed in the rejections above, Sang et al.

discloses that the switching subsystem 42 (shown in detail in Figure 3), which

corresponds to the claimed "arbitrator", issues a grant for the dequeuing logic 76 of the

transmit port to initiate a direct memory access to transfer data from the external

memory 36 to the destination port (See column 7 line 51 to column 8 line 12 of Sang et

al.). This direct memory access grant issued by the switching subsystem 42 means that

the switching subsystem 42 arbitrates direct connection of the external memory 36 with

the transmit FIFO of the MAC module identified as the destination port. Therefore, the

switching subsystem of Sang et al. meets the claim 1 limitation of "an arbitrator …

arbitrates direct connection of the memory array storage area associated with the MAC

unit that receives the incoming data packet to the MAC unit identified as the destination

port, thereby facilitating direct transfer of the packet payload of the incoming data packet to the destination port".

Conclusion

8.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
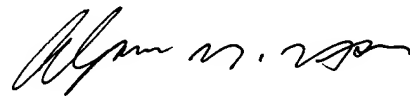
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason E Mattis whose telephone number is (571) 272-3154. The examiner can normally be reached on M-F 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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